CLAIMS

What is claimed is:

1. A single-die integrated circuit for switching among a plurality of transmission ports and a plurality of receiver ports, comprising:

a transmitter switching section having a plurality of transmission ports, transmitter control circuitry operable to switch a selected one of the plurality of transmission ports to a transmission node; and

a receiver switching section having a plurality of receiver ports, receiver control circuitry operable to switch a selected one of the plurality of receiver ports to the transmission node.

2. The integrated circuit of Claim 1, wherein the receiver switching section includes at least two cascaded stages, a first cascaded stage controllable to switch the transmission node to a receiver node, a second cascaded stage controllable to switch the receiver node to a selected one of the plurality of receiver ports.

3. The integrated circuit of Claim 1, and further comprising an antenna port coupled to the transmission node.

4. The integrated circuit of Claim 1, wherein, for each transmission port, the transmitter switching section includes a series field effect transistor (FET) switching topology operable to couple the last said transmission port to the transmission node.

5. The integrated circuit of Claim 4, wherein each series FET switching topology comprises a plurality of FETs having current paths coupled in series with each other.

6. The integrated circuit of Claim 5, wherein each series FET switching topology includes a first one of the FETs proximate the respective transmission port, the first FET having a current path with a first end coupled to the transmission port and a gate, a feed-forward capacitor coupled between said first end and the gate of the coupled and a gate.

7. The integrated circuit of Claim 5, wherein each FET switching topology includes a last FET having a current path and a gate, a first end of the current path coupled to the

transmission node, a feed-forward capacitor coupled from the gate to the first end of said current path.

8. The integrated circuit of Claim 5, wherein, for at least one of the FET switching topologies, a bypass resistor is coupled across at least two of the current paths of the plurality of FETs.

9. The integrated circuit of Claim 4, wherein at least one of the FET switching topologies includes at least one FET having a plurality of contiguous source regions interdigitated with a plurality of contiguous drain regions, a sinuous gate formed to wind between the source regions and the drain regions.

10 A single-die multiband switch for wireless communication, comprising:

an antenna port;

a plurality of transmitter ports, for each transmitter port a switching topology operable to switch the last said transmitter port to the antenna port; and

a plurality of receiver ports, for each receiver port a switching topology operable to switch the last said receiver port to the antenna port.

11. The switch of Claim 7, wherein at least one of the switching topologies comprises a plurality of series-connected field effect transistors, a control signal for said at least one switching topology controlling said at least one switching topology to selectively connect or isolate a respective transmitter or receiver port from the antenna port.

12. The switch of Claim 7, wherein at least one of the switching topologies comprises at least one interdigitated field effect transistor having a plurality of elongated contiguous drain regions, a plurality of elongated contiguous source regions interdigitated with the drain regions, an elongated sinuous channel region spacing apart the drain regions from the source regions, and a gate overlying the channel region to switch the interdigitated field effect transistor between an ON and an OFF state.

13. The switch of Claim 7, wherein the die has an area, the transmitter port switching topologies occupying an area on the die which is substantially larger than the receiver port switching topologies.

14. The switch of Claim 7, and further including at least one multiple-stage switching topology, a first stage of the multiple-stage switching topology selectively connecting or isolating the antenna port from the multiple-stage switching topology, a last stage of the multiple-stage switching topology selectively connecting or isolating a plurality of other ports from the multiple-stage switching topology.

15. The switch of Claim 11, wherein said other ports are receiver ports.

16. The switch of Claim 12, wherein said last stage includes, for each receiver port, a signal path FET having a current path controllable to connect the receiver port to an intermediate node, said first stage operable to connect the intermediate node to the antenna port.

17. The switch of Claim 16, wherein each said signal path FET has a gate to which a control signal is applied, a shunt FET having a drain coupled to the gate, a source coupled to ground and operable to enhance isolation of the receiver port from the intermediate node when the signal path FET is in an OFF state.

18. A single-die transmitter/receiver integrated switching circuit, comprising:

a plurality of transmitter ports;

a plurality of receiver ports;

at least one antenna port;

a plurality of integrated circuit switching elements controllable to connect one of the transmitter ports or one of the receiver ports to the antenna port while isolating the remaining ones of the transmitter and receiver ports from the antenna port, at least one of the plurality of transmitter ports and the plurality of receiver ports being at least three in number, at least some of the integrated circuit switching elements arranged in cascaded fashion in order to reduce signal insertion loss.

19. The integrated switching circuit of Claim 14, wherein there are at least three receiver ports, any one receiver port selectably switched to be connected to the antenna port through at least two cascaded stages of integrated circuit switching elements.

20. The integrated switching circuit of Claim 14, wherein the integrated circuit switching elements are field effect transistors.

21. A method of switching one of a plurality of transmitters and a plurality of receivers to a transmitter/receiver antenna, comprising the steps of:

connecting each transmitter to a respective one of a plurality of transmitter ports formed on a single integrated circuit die;

connecting each receiver to a respective one of a plurality of receiver ports formed on the die;

controlling a selected one of a plurality of switching topologies each associated with a respective one of the transmitter and receiver ports to connect a respective selected one of the transmitter and receiver ports to an antenna port formed on the die; and

controlling other ones of the switching topologies to isolate others of the transmitter and receiver ports from the antenna port.

22. The method of Claim 17, and further including the steps of:

arranging at least some of the switching topologies in cascaded stages including a first stage coupled to the antenna port and a last stage coupled to a plurality of the transmitter or receiver ports;

connecting a selected one of the last said transmitter or receiver ports to the antenna ports by switching on the first stage, and switching on a switch associated with said selected one of the last said transmitter or receiver ports wherein the last said switch is a portion of the last stage; and

switching off the remaining switching topologies and other switches in the last stage.

23. The method of Claim 18, wherein said step of controlling a selected one of the switching topologies includes the step of switching a plurality of series-connected switching transistors to an ON state.

24. The method of Claim 21, and further including the steps of:

switching at least one signal path transistor to an ON state to pass a signal from an associated one of the receiver or transmitter ports through a current path of the signal path transistor;

turning off a shunt transistor having a drain connected to a gate of the signal path transistor so as to isolate the gate from ground;

for at least one nonselected receiver or transmitter port, switching an associated signal path transistor to an OFF state; and

for said at least one nonselected receiver or transmitter port, turning on an associated shunt transistor having a drain connected a gate of the associated signal path transistor, such that the last said gate is coupled to ground and such that the isolation of the nonselected receiver or transmitter port is enhanced.